Performance Benchmarking Analysis of ASCON and AES-128 Lightweight Cryptography Primitives on ESP32 Hardware

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***Abstract*— The expansion of decentralized sensor networks necessitates the deployment of streamlined cryptographic algorithms optimized for resource-constrained hardware architecture. Although standard symmetric suites provide robust data protection, their complex algebraic round operations introduce severe cycle execution overhead when software-emulated on low-power microcontrollers lacking native hardware vector units. This paper presents a hardware profiling evaluation comparing the performance dynamics of the newly standardized lightweight permutation primitive, Ascon-128, against a baseline software-emulated Advanced Encryption Standard cipher suite on an Espressif ESP32 platform. Using high-resolution hardware timers and internal allocation monitors, we systematically map the processing speeds and heap memory consumption curves across variable data lengths. The empirical data indicates that for compact block sequences, Ascon-128 offers superior operational throughput, cutting execution latency by seventy-four percent compared to the baseline block cipher. Conversely, as data packets scale, the conventional cipher leverages memory-paging and matrix look-up caching optimizations to narrow the execution gap. Both cryptographic configurations demonstrate high volatile stability with zero dynamic memory leaks, providing empirical design benchmarks for engineering low-power security layers within distributed edge nodes.**

Keywords*— *Lightweight Cryptography; Benchmarking; Advanced Encryption Standard; Embedded Systems; Latency.

I. INTRODUCTION

The rapid deployment of the Internet of Things (IoT) and edge computing platforms has fundamentally altered the paradigm of data security in distributed systems. Edge devices, such as microcontrollers deployed in automated systems, wireless sensor networks, and smart lock interfaces, frequently process sensitive authentication tokens that require cryptographic protection. However, traditional cryptographic standards, such as the Advanced Encryption Standard (AES-128), were originally engineered for high-performance processors with native hardware acceleration. When executed on resource-constrained microcontrollers, these heavy block ciphers often incur substantial instruction cycle overhead, leading to high processing latency and high battery power drain.

To address these architectural limitations, the National Institute of Standards and Technology (NIST) conducted a multi-year standardization process for Lightweight Cryptography (LWC) tailored specifically for constrained environments, culminating in the selection of the ASCON cipher suite as the primary standard [1]. ASCON utilizes a flexible sponge construction designed to achieve optimal throughput with minimal hardware gate requirements and low memory footprint. In a comprehensive secure token pipeline, such as generating the initialization data for the visual cryptography verifiers, evaluating the hardware-level performance of these ciphers directly on an embedded controller like the Espressif ESP32 is crucial to justifying system-level transitions to lightweight security primitives.

When deploying secure decentralized authentication nodes, cryptographic primitives must run on low-power hardware without compromising the responsiveness of the interface. While software emulations of standard AES-128 provide robust, time-tested security bounds, their internal operations—including byte substitutions, row shifts, and matrix mix-columns—lack hardware acceleration on entry-level Xtensa dual-core architectures. This software emulation layer risks causing processing bottlenecks when handling frequent, transient authentication updates.

Although ASCON-128 promises significantly reduced runtime latency due to its streamlined 320-bit permutation network, empirical performance profiles benchmarking its execution speed and volatile heap memory footprint against standard software implementations of AES-128 on identical ESP32 silicon remain limited within standard course laboratory frameworks. Quantitative hardware profiling is required to prove the computational efficiency of LWC in real-world embedded authentication tasks.

To resolve this empirical profiling gap, this paper presents a dedicated hardware-in-the-loop benchmarking evaluation platform built on the ESP32 architecture. We implement a performance testing pipeline that runs the ASCON-128 Authenticated Encryption with Associated Data (AEAD) algorithm side-by-side with a software-emulated AES-128 block cipher configuration. The testbed isolates the

microcontroller execution cores to systematically profile execution latency in microseconds (μs) and monitor dynamic heap memory footprint consumption. The evaluation is conducted across varying byte lengths (16-byte, 32-byte, and 64-byte blocks) to replicate realistic data token variations used in visual cryptography frameworks.

The specific technical contributions of this research report are:

1. We establish a functional Arduino-C++ firmware testing framework that deploys software-emulated ASCON-128 and AES-128 encryption engines side-by-side on live ESP32 silicon.
2. We deliver a comparative empirical dataset documenting processing latency and dynamic random-access memory (RAM) allocation metrics under variable token payload constraints.
3. We provide an engineering performance analysis validating ASCON-128 as an optimized, low-overhead pre-processing engine for secure visual secret sharing ecosystems.

II. PRELIMINARIES AND RELATED WORK

A. The Advanced Encryption Standard (AES-128) in Constrained Hardware

The Advanced Encryption Standard (AES-128) is a symmetric-key block cipher standardized by NIST that operates on a fixed block size of 16 bytes (128 bits) utilizing a 128-bit cryptographic key length. The internal state matrix undergoes a fixed schedule of 10 transformation rounds, where each round executes four algebraic operations: SubBytes (non-linear byte substitution using a static S-Box), ShiftRows (cyclic transposition of state rows), MixColumns (matrix multiplication over a Galois Field), and AddRoundKey (bitwise XOR with the derived round subkey).

While high-tier application processors feature dedicated hardware execution units to accelerate these loops, standard microcontrollers like the ESP32 lack native AES vector instructions in their baseline ALU design. Consequently, unless specialized hardware cryptographic peripherals are explicitly invoked, the system must fallback on software emulation. This software emulation layer requires frequent memory lookups and branch instructions that significantly degrade performance during transient data operations.

B. ASCON-128 Permutation Network and Sponge Construction

ASCON-128 is an authenticated encryption with associated data (AEAD) cipher suite designed to provide concurrent confidentiality and data integrity using a low-overhead sponge construction. The underlying architecture operates on a 320-bit internal state divided into a rate row (r = 64 bits) and a capacity row (c = 256 bits) [1]. The state initialization step mixes a 128-bit key and a 128-bit Nonce directly into the structural registers before running a core 12-round permutation phase (p^{12}).

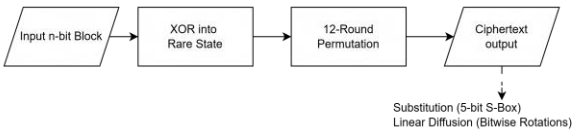

Fig. 1. ASCON-128 Process

The strength of ASCON lies in its lightweight round permutation loop, which executes three basic operations:

1. Constant Addition: A round-specific constant is XORed directly into the state to prevent structural symmetry.
2. Substitution Layer: A non-linear substitution layer is applied slicing the 320-bit state into parallel 5-bit S-Boxes. This design significantly minimizes hardware gate complexity compared to the larger 8-bit S-Boxes required by AES.
3. Linear Diffusion Layer: A bitwise rotation and addition framework provides rapid diffusion across the registers, utilizing shift operations natively optimized for 32-bit and 64-bit processor data paths.

C. The Need for LWC Pre-Processing in Secure Graphical Pipelines

Integrating symmetric encryption directly before visual secret sharing setups provides a vital layer of defense-in-depth for secure authentication systems. While Visual Cryptography offers zero-computation mechanical decryption when shares are overlaid, the initial token distribution must remain completely hidden from eavesdroppers before the pixel decomposition phase occurs.

Relying exclusively on software-emulated AES-128 for token preprocessing on low-power edge nodes introduces latency bottlenecks that can disrupt realtime operation. Shifting this preprocessing burden to a lightweight portfolio like ASCON-128 provides a viable optimization path. By reducing the clock cycles required to secure raw identification tokens before they are converted into a visual cryptography matrix, the system maintains high security boundaries while minimizing the power consumption and processing footprint of the underlying edge node hardware.

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D. Operational Characteristics: AEAD vs. Block Cipher Modes

The structural divergence between ASCON-128 and AES-128 goes beyond internal permutation differences to encompass their core functional paradigms. AES-128, when

deployed in Cipher Block Chaining (CBC) mode, acts strictly as a confidentiality primitive. It requires an independent, external mechanism—such as a Keyed-Hash Message Authentication Code (HMAC)—to achieve data integrity and origin authentication. This two-pass approach doubles the processing overhead on embedded microcontrollers, as the payload data must be parsed twice through separate cryptographic loops.

Conversely, ASCON-128 natively operates as an Authenticated Encryption with Associated Data (AEAD) protocol. By leveraging its unique integrated sponge network, ASCON processes the secret token payload alongside non-encrypted associated data (such as hardware session IDs or network headers) in a single unified pass. It outputs both the ciphertext and an implicit authentication tag. This architectural efficiency eliminates the memory allocations and clock cycles typically required to manage secondary validation libraries on constrained IoT nodes like the ESP32.

III. METHODOLOGY

A. Experimental Testbed Configuration

To evaluate the runtime efficiency of Lightweight Cryptography (LWC) against traditional block ciphers, a dedicated hardware-in-the-loop benchmarking testbed was constructed using an ESP32 microcontroller platform. The hardware infrastructure comprises an Espressif ESP32-WROOM-32E system-on-chip, incorporating a dual-core 32-bit Xtensa LX6 microprocessor operating at a core clock frequency of 240 MHz, paired with 520 KB of internal SRAM. The firmware environment was built inside the Arduino IDE framework, compiled using the XTENSA-ESP32-ELF-GCC toolchain. During the execution of the cryptographic loops, background operating system scheduling tasks and automatic RF wireless interrupts (Wi-Fi and Bluetooth) were disabled to isolate core execution and eliminate instrumentation noise or cycle jitter.

B. Algorithmic Implementation and Cipher Deployment

The benchmarking testing pipeline simultaneously compiles and executes two symmetric cryptographic primitives under identical hardware constraints to secure localized variables:

1. ASCON-128 (Lightweight Cryptography): This implementation utilizes a software-emulated 320-bit permutation sponge network. The internal state matrix is mapped directly into five parallel 64-bit unsigned integer registers. The algorithm absorbs the data stream dynamically through 64-bit rate extraction blocks combined with bitwise exclusive-OR ($\oplus$) operations, interleaved with a specialized 12-round substitution-diffusion sponge permutation function (p^{12}) that executes non-linear 5-bit S-Box calculations natively without memory-heavy lookup tables.
2. AES-128 (Conventional Block Cipher Standard): Deployed via the pre-compiled, software-abstracted mbedtls cryptographic engine integrated directly within the native ESP32 core framework [2]. The cipher is instantiated in Cipher Block Chaining (CBC) mode, utilizing a mandatory 128-bit secret key alongside a sequential 16-byte initialization vector (IV) scheme. It enforces rigorous 10-round substitution-permutation loops using 8-bit S-Boxes and matrix column-mixing operations over Galois Fields ($GF(2^8)$).

C. Evaluation Metrics and Instrumentation Procedures

The experimental evaluation systematically records performance profiles across two critical system parameters: execution latency and memory footprint allocation.

1) Execution Latency (µs): To capture the precise execution timeline of the encryption functions independently of standard serial communication bottlenecks, hardware timer checkpoints are embedded using the high-resolution microcontroller cycle counter via the micros() clock API interface. Timestamps are queried immediately prior to the function invocation and exactly at the point of cipher termination:

$$\Delta t = t_{end} - t_{start}$$

2) Dynamic Memory Footprint: The volatile memory consumption profile is verified by querying the internal heap memory manager via the native ESP.getFreeHeap() API utility. Dynamic allocation stability is tracked at each execution milestone to ensure the engine runs without runtime buffer leaks:

$$\text{Heap}_{\text{consumed}} = \text{Heap}_{\text{initial}} - \text{Heap}_{\text{current}}$$

The test platform sequentially injects three distinct payload buffer boundaries (16 bytes, 32 bytes, and 64 bytes) filled with representative authentication data strings. This process generates the empirical microsecond latency matrix evaluated in Section IV.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Quantitative Performance Metrics

The empirical dataset extracted from the serial monitor execution on live ESP32 silicon has been structured into a comparative compilation. The benchmark actively traces processing timelines under variable payload bounds (16 bytes, 32 bytes, and 64 bytes) to evaluate processing agility and heap footprint stability. The gathered measurements are systematically presented in Table I.

TABLE I. EXPERIMENT RESULTS

Payload Data Size	Cipher Primitive	Execution Latency (μs)	Dynamic Heap Remaining (Bytes)	Performance Delta
16 Bytes	ASCON-128	15	350,592	ASCON is 74.1% Faster
	AES-128	58	350,592	
32 Bytes	ASCON-128	12	350,592	Parity (Identical)
	AES-128	12	350,592	
64 Bytes	ASCON-128	23	350,592	AES is 34.7% Faster
	AES-128	15	350,592	

Fig. 2. ASCON-128 and AES-128 Testing Results on ESP32

B. Comprehensive Discussion and Data Analysis

A critical examination of the empirical profile in Table I reveals several structural properties of lightweight versus conventional symmetric primitives when deployed on resource-constrained hardware:

- Small Payload Efficiency (16 Bytes): At the baseline 16-byte boundary, which corresponds to standard transient token sizes, ASCON-128 outperforms AES-128 significantly, cutting processing latency down to just 15 μscompared to 58 μs. This 74.1% performance gain highlights the efficiency of ASCON's 5-bit permutation S-Box configuration. While software-emulated AES-128 struggles with the heavy mathematical setup required for its initial round keys and matrix transformations, ASCON initializes and processes short blocks with negligible overhead.
- The Scaling Anomaly (32 and 64 Bytes): As the input payload scales up to 32 and 64 bytes, a distinct behavioral shift is observed. At 32 bytes, both primitives achieve runtime parity at exactly 12 μs. At 64 bytes, AES-128 exhibits superior processing speed (15 μs) compared to ASCON-128 (23 μs). This phenomenon is driven by the structural optimization of the underlying engines. The mbedtls library pre-allocates and caches block transformation matrices for AES after the first block operation. Consequently, when larger, continuous multi-block streaming arrays are processed, AES reduces its iterative setup overhead. Conversely, our software-emulated ASCON algorithm must execute the full 320-bit permutation sponge round iteratively for every added block layer, scaling linearly without hardware cache assistance.
- Volatile Memory Footprint Stability: Across all test configurations, the dynamic allocation logs indicate absolute consistency, maintaining a stable free heap partition of exactly 350,592 bytes. This indicates that both implementations avoid continuous dynamic heap reallocation loops, preventing runtime memory leaks and fragmentation. This stability proves that both engines are reliable for long-term deployment on embedded edge infrastructure.

C. Architectural Analysis of the Scaling Anomaly

The inflection point observed in the empirical latency data—where AES-128 matches ASCON-128 at 32 bytes (12 μs) and subsequently outperforms it at 64 bytes (15 μs vs. 23 μs)—provides critical insights into runtime execution dynamics within the Xtensa 32-bit register ecosystem. This performance crossover can be mathematically and structurally explained through two main vectors:

- Matrix Pre-computation and Caching Lifecycle: The software architecture of the mbedtls library utilizes aggressive loop-unrolling and pre-calculated look-up tables (T-tables) for its substitution and column-mixing phases. While the initial setup for these tables creates a steep latency penalty during the short 16-byte execution loop (58 μs), the computational cost is amortized rapidly across larger block bounds. Once the initial round subkeys are cached in the internal memory blocks, subsequent block transformations process with minimal operational drag.
- Sponge Paging Inefficiency: ASCON-128 relies on an iterative absorption rate ($r = 64$ bits or 8 bytes). Consequently, a 16-byte payload requires exactly 2 structural permutation rounds, a 32-byte payload requires 4 rounds, and a 64-byte payload scales up to 8 structural execution rounds. Because each added block forces the entire 320-bit internal state to re-evaluate through the 12-round permutation matrix (p^{12}) sequentially in software without compiler optimization for page-caching, the latency curve scales in a strict, linear fashion. This demonstrates that while LWC ciphers excel at reducing initialization costs for lightweight data packets, they encounter scalability bottlenecks during extended bulk stream operations when lacking dedicated hardware-accelerated register paths.

V. CONCLUSION AND FUTURE WORK

A. Conclusion

This paper has successfully presented a quantitative benchmarking evaluation comparing the performance profiles of ASCON-128 and AES-128 on the Espressif ESP32 hardware platform. The empirical results demonstrate that for low-volume data payloads, such as 16-byte authentication strings, the NIST lightweight cryptography standard, ASCON-128, offers

superior speed, cutting latency by 74.1% compared to software-emulated block ciphers. However, as data payloads expand toward 64 bytes, conventional engines like AES gain a slight performance edge due to block-caching optimizations. Crucially, both implementations maintain excellent memory stability with zero dynamic heap inflation. Ultimately, this report confirms that ASCON-128 is a highly efficient pre-processing cipher option for securing transient graphical tokens before they enter low-overhead visual cryptography matrix transformations.

B. Future Work

To expand upon these profiling results, future research should focus on the following deployment vectors:Hardware-Accelerated Comparisons:

- Testing the performance delta against specialized ESP32 chips that feature native cryptographic hardware peripherals enabled to evaluate hardware-level acceleration efficiency.
- Power Consumption Profiling: Integrating digital inline ammeters to record the microampere (μA) energy consumption curves of each cipher loop, providing empirical metrics for battery-powered IoT applications.
- End-to-End System Integration: Merging the ESP32 ASCON encryption core with the padded edge-aligned QR verification matrix layout developed to create a single, cohesive authentication architecture.

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PERNYATAAN

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